MLSI-DR11B

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MLSI-DR11B

DIRECT MEMORY ACCESS MODULE

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INTRODUCTION

The MLSI-DR11B Direct Memory Access Module is an interface for the direct-memory-access transfer of data between a Digital Equipment Corporation (DEC) LSI-11 computer memory, and the user's peripheral device (figure 1).

The MLSI-DR11B consists of a single quad module. The MDB module is a unibus version of the MDB-DR11B and can be converted to simulate a DRV11B. If configured as a DRV11B, DRV11B software can be used.

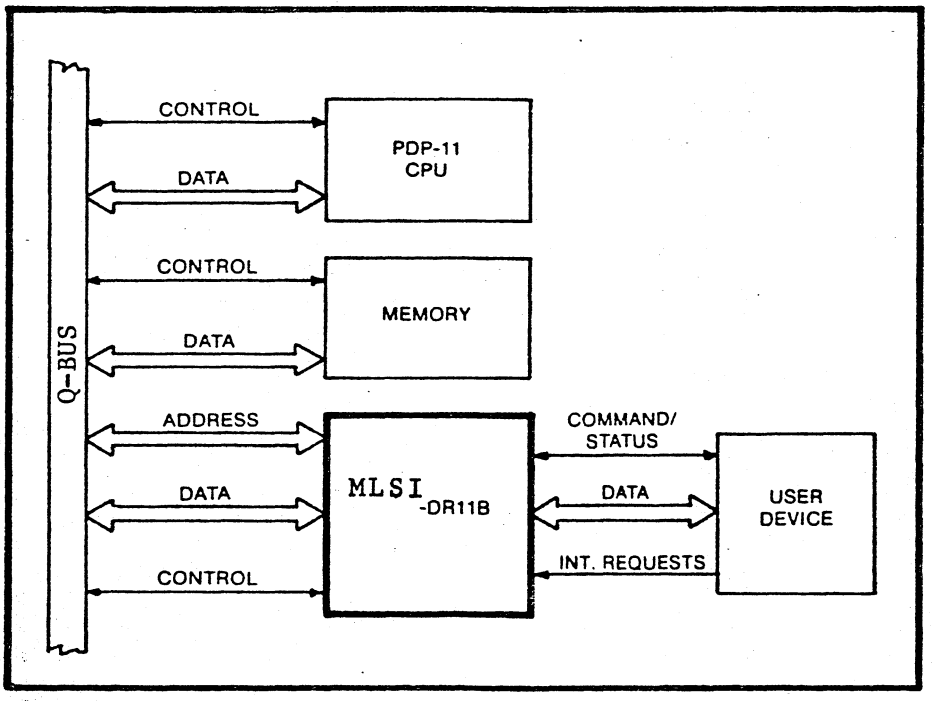


Figure 1. System Block Diagram

Logic on the module includes the following facilities:

a. bus drivers and receivers;

b. four registers, as follows:

Data Register
Word Count Register
Address Register
Command/Status Register;

c. A multiplexer to select the bus address, word count, input data, or command/status information onto the Q-BUS;

d. logic to decode the received device address; and

e. interrupt and bus master control logic.

Operation is always begun under program control which does the following:

a. loads the required word count into the Word Count Register;

b. specifies the starting memory address or bus address at which the block transfer is to begin; and

c. loads function bits into the Command/Status Register.

The user device responds to the function bits by setting-up controls to the DR11B. If the user device is to receive data, the DR11B performs a DATI operation, loading its data register with information at the specified bus address. Outputs of the Data Register are presented to the user device.

If the user device is to send data to the memory, the DR11B performs a DATO operation, transferring data words from the user device to the specified bus address. Note that input data is not buffered and must be retained for the entire Q-BUS transfer.

Data and control signals at the MLSI-DR11B/user interface are at standard TTL levels.

PHYSICAL DESCRIPTION

The MLSI-DR11B module is a quad module fitting into one slot in the system's assembly. The interface to the Q-BUS is through the assembly backplane. The module is connected to the user device through two 40-pin Berg connectors, J1 and J2.

The MLSI-DR11B is powered by the +5V dc supply at the systems assembly, and requires 2.4 amperes from that supply.

INSTALLATION

The following paragraphs contain instructions and information for installing the MLSI-DR11B module, and for installing or removing jumpers that configure the module for its application.

Installing Module

Plug the module into any available slot in the LSI-11 BackPlane

Cabling

The module has two Berg connectors for the user device interface. Cables from the device may be brought directly to these connectors.

Jumper Connections and Switch Settings

Certain jumper connections and switch settings may be prepared on the module in order to configure the module for its application. The module is furnished with certain preferred configurations strapped by printed circuit etch. To change configurations, cut etch and/or install wire jumpers as required.

Device Address

Set device address by using switches on DIP module as indicated in Table 1. Jumper 3J-H should be installed.

Table 1 Device Address Selection

DIGIT W		DIGIT X		DIGIT Y		DIGIT Z	
SW.#	VALUE	SW.#	VALUE	SW.#	VALUE	SW.#	VALUE
9B		9B | 11B		11B		11B	
1 2 3 4 5 6		7 | 1 2		3 4 5		6 7 8	
● ● ● ● ● ●	6	● ● ●	0	● ● ●	0	● ● ●	0
● ● ● ● ● o	7	● ● o	1	● ● o	1	● ● o	1
		● o ●	2	● o ●	2	● o ●	2
		● o o	3	● o o	3	● o o	3
		o ● ●	4	o ● ●	4	o ● ●	4
		o ● o	5	o ● o	5	o ● o	5
		o o ●	6	o o ●	6	o o ●	6
		o o o	7	o o o	7	o o o	7

o = open ● = close (ON) Address = 7WXYZ0

Address assignments determined by standard DEC software are as follows:

No. of DR11B Module	Register Address
First	772410 - 772416
Second	772430 - 772436
Third	772450 - 772456
Fourth	772470 - 772476

Set vector address by using switches on DIP module in location 10B. Normal interrupt vector is 124_8.

Interrupt Vector Address Selection

DIGIT X		DIGIT Y		DIGIT Z	
SW.#	VALUE	SW.#	VALUE	SW.#	VALUE
1 2 3		4 5 6		7 8	
● ● ●	0	● ● ●	0	● ●	0
● ● o	1	● ● o	1	o ●	4
● o ●	2	● o ●	2		
● o o	3	● o o	3		
o ● ●	4	o ● ●	4		
o ● o	5	o ● o	5		
o o ●	6	o o ●	6		
o o o	7	o o o	7		

o = open ● = close (ON) Address=XYZ

Special Jumpers

(1) J-H for DR11B Version
(1) J-K for DR11BV Version
(2) J-K for DR11B Version (NORMAL)
(2) J-H for DR11BV Version
(8) J-H for DR11B Version (NORMAL)
(8) J-K for DR11BV Version

Bus Address Overflow Control
(4) J-K and (5) J-H (NORMAL)

If your application permits disregarding 32K boundary, jumpers may be reconfigured so that each 32K overflow simply increments the Extended Bus Address count, and sets READY and ERROR only when the address has overflowed the limit of system addressing. To select this mode of operation cut etch jumpers (4) J-K and (5) J-H and connect wire jumpers to (4) J-H and (5) J-K.

BBS7-To strap high order bits to BBS7 on DATI Function, jumper (6) J-H and (7) J-K and remove jumper (7) J-H (DR11BV Version uses high order bits to BBS7 on DATI FUNCTION).

P1 AND P2 PINOUT ARE AS FOLLOWS:

MLSI-DR11B			DEC DRV11B		
P1-1	D15	IN	J2-VV	D15	IN
-2	D00	IN	-UU	D00	IN
-3	D14	IN	-TT	D14	IN
-4	D01	IN	-SS	D01	IN
-5	D13	IN	-RR	D13	IN
-6	D02	IN	-PP	D02	IN
-7	D12	IN	-NN	D12	IN
-8	D03	IN	-MM	D03	IN
-9	D11	IN	-LL	D11	IN
-10	D04	IN	-KK	D04	IN
-11	D10	IN	-JJ	D10	IN
-12	D05	IN	-HH	D05	IN
-13	D09	IN	-FF	D09	IN
-14	D06	IN	-EE	D06	IN
-15	D08	IN	-DD	D08	IN
-16	D07	IN	-CC	D07	IN
-17	COI		-BB	GND	
-18	AOOI		-AA	GND	
-19	ATTN		-Z	GND	
-20	GND		-Y	GND	
-21	BA INC ENB		-X	GND	
-22	GND		-W	GND	
-23	INIT V20		-V	FNCT 10	
-24	GND		-U	GND	
-25	BUSY		-T	C1I	
-26	GND		-S	GND	
-27	C1I		-R	FNCT 20	
-28	GND		-P	GND	
-29	STATUS C		-N	COI	
-30	GND		-M	GND	
-31	STATUS B		-L	FNCT 30	
-32	GND		-K	FNCT 30	
-33	SINGLE CYCLE		-J	BA INC ENB	
-34	GND		-H	GND	
-35	STATUS A		-F	AOOI	
-36	GND		-E	GND	
-37	GDO		-D	ATTN	
-38	GND		-C	GND	
-39	CYCLE REQ		-B	BUSY	
-40	GND		-A	GND	

MLSI-DR11B		
P2-1	D15	OUT
-2	D00	OUT
-3	D14	OUT
-4	D01	OUT
-5	D13	OUT
-6	D02	OUT
-7	D12	OUT
-8	D03	OUT
-9	D11	OUT
-10	D04	OUT
-11	D10	OUT
-12	D05	OUT
-13	D09	OUT
-14	D06	OUT
-15	D08	OUT
-16	D07	OUT
-17	GND	
-18	GND	
-19	INITO	
-20	GND	
-21	WC INC ENB	
-22	GND	
-23	READYO	
-24	GND	
-25	P.U.	
-26	GND	
-27	FNCT 10	
-28	SNL	
-29	FNCT 10	
-30	GND	
-31	FNCT 20	
-32	GND	
-33	FNCT 30	
-34	GND	
-35	FNCT 30	
-36	GND	
-37	CREQB	
-38	GND	
-39	END CYCLE	
-40	GND	

DEC DRV11B		
J1-VV	D15	OUT
-UU	D00	OUT
-TT	D14	OUT
-SS	D01	OUT
-RR	D13	OUT
-PP	D02	OUT
-NN	D12	OUT
-MM	D03	OUT
-LL	D11	OUT
-KK	D04	OUT
-JJ	D10	OUT
-HH	D05	OUT
-FF	D09	OUT
-EE	D06	OUT
-DD	D08	OUT
-CC	D07	OUT
-BB	GND	
-AA	GND	
-Z	GND	
-Y	GND	
-X	GND	
-W	GND	
-V	STATUS C	
-U	GND	
-T	STATUS C	
-S	GND	
-R	STATUS B	
-P	GND	
-N	INITO	
-M	GND	
-L	STATUS A	
-K	SINGLE CYCLE	
-J	WC INC ENB	
-H	GND.	
-F	READYO	
-E	GND	
-D	INIT V20	
-C	GND	
-B	CYCLE REQ	
-A	GND	

REGISTERS

There are four registers available to the Q-BUS. Each register is described in the following paragraphs.

Data Register

The 16-bit Data Register is used both to read, and write, data as follows:

a. Write Data. The register stores the output data word for presentation to the user device. The register is loaded under program control.

b. Read Data. A data word from the user device is transferred to the Q-BUS without buffering. That is, the user device must hold data on the lines until it is read under program control or transferred directly to memory.

The preferred Data Register address is 772416.

Word Count Register

The Word Count Register is a 16-bit read/write register. It is loaded from the Q-BUS, under program control, with the 2's-complement of the number of words to be transferred, and normally is incremented one count towards zero as each word is transferred. Incrementing may be inhibited by a WC INC ENB signal from the user device.

When the word count reaches zero, the READY bit is set in the command/status word to stop the bus cycle.

The preferred Word Count Register address is 772410.

Bus Address Register

The Bus Address Register is a 15-bit register, as bit 0 is furnished by the user device. The contents of the register are used, along with bits XBA16 and XBA17 (in the Command/Status Register) to specify the bus address.

The Bus Address Register is normally incremented after each word to be transferred, advancing the address to the next word location. The user device may inhibit incrementing by asserting BA INC ENB.

The ERROR bit is set in the Command/Status Register if the address overflows (changes from all-"1's to all-"0's"). The error (BAOF) is cleared either by INIT or by loading a new number into the Bus Address Register.

The preferred Bus Address Register address is 772412.

Command/Status Register

The contents of the Command/Status Register are commands to control the user device, and bits giving user device status to the Q-BUS. Table 2 lists and defines bits in the Command/Status Register.

The preferred Command/Status Register address is 772414. Figure 3 shows the contents of the Command/Status Register.

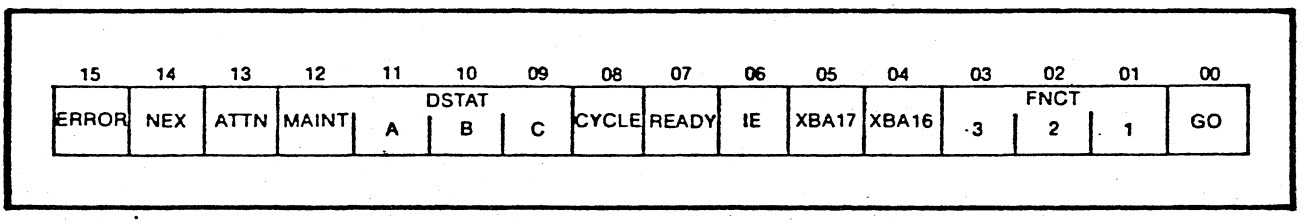


Figure 3. Contents of Command/Status Register

Table 2. Command/Status Bits

Bit	Name	Description and Effect
15	ERROR (read only)	a. Indicates error as follows: 1. NEX (bit 14), or 2. ATTN (bit 13), or 3. Interlock error (module/connector discontinuity), or 4. Bus address overflow (BAOF) as bus address changes from all-"1's" to all-"0's". b. Sets READY (bit 7) and causes interrupt if IE (bit 6) has been set. c. ERROR is cleared by clearing all error conditions, as follows: 1. Module is seated in connector. 2. Bus address is cleared or reloaded. 3. Bit 14 is loaded with a "0". 4. Bit 13 is cleared by the user device.
14	NEX (read)	a. Non-existent Memory. Indicates that the module, acting as bus master, failed to receive a RPLY response within 20 micro-seconds after asserting SACK. b. NEX sets ERROR bit. c. Cleared by INIT or by loading "0".
13	ATTN (read only)	a. Attention. Shows state of user device ATTN signal. b. Sets ERROR for device-initiated interrupt. c. Set and cleared only by user device.
12	MAINT (read/write)	a. Maintenance. Used to enable execution of diagnostic programs. b. Cleared by INIT.

Table 2. Command/Status Bits (cont'd)

Bit	Name	Description and Effect
11 10 09	DSTATA DSTATB DSTATC (read only)	a. Device Status. Indicate state of user-designated DSTATA, DSTATB, and DSTATC signals. b. Set and cleared only by user device.
08	CYCLE (read/write)	a. If set when GO is issued, enables an immediate bus cycle. b. Cleared by INITI, or start of bus cycle.
07	READY (read only)	a. Indicates the MLSI-DR11B is able to accept a new command. b. Set by INIT or ERROR, or by word count overflow. c. Cleared by GO. d. If bit 6 is set, READY causes an interrupt, forcing module to release the Q-BUS.
06	IE (read/write)	a. Interrupt Enable. Enables either ERROR or READY to set an interrupt. b. Cleared by INIT.
05 04	XBA17 XBA16 (read/write)	a. Extended Bus Address. Along with contents of Bus Address Register, specify address for indirect memory transfers. b. Cleared by INIT. c. Bits XBA17 and XBA16 are not incremented when Bus Address Register overflows, but ERROR is set.
03 02 01	FNCT3 FNCT2 FNCT1 (read/write)	a. Function. Bits available to user device for assignment by user. b. Cleared by INIT.
00	GO (write only)	a. Causes MLSI-DR11B to signal user device that a command has been issued. b. Clears READY.

USER DEVICE INTERFACE

Signals at the user device interface are at standard TTL levels. Table 3 lists and defines signals at the user device interface. Unless otherwise stated, logic is asserted at the high level.

Table 3. User Device Interface Terms

Signal	Description
Inputs to MLSI-DR11B from User Device	
DAT100-DAT115	Sixteen data lines. Data must be held until transferred to memory in a DATO cycle.
C1 CONTROL IN C0 CONTROL IN	Two signals specify type of Q-BUS cycle to be performed, DATI, DATØ, AND BYTE.
CYCLE REQ A, CYCLE REQ B	Either signal sets CYCLE bit to initiate bus request and subsequent Q-BUS cycle. Must be pulsed positive for at least 100 nanoseconds (negative-going transition is active).
WC INC ENB	**Word Count Increment Enable.** To permit counting each bus cycle, this line must be held high.
BA INC ENB	**Bus Address Increment Enable.** To permit the Bus Address Register to increment following each bus cycle, this line must be held high.
A00IN	**Bus Address Bit 00.** Used as bit 0 of the Bus Address Register. For sequential word addressing A00 is held low. The line may be controlled to permit byte addressing.
DSTATA, DSTATB, DSTATC	**Device Status Bits.** User-assigned status signals. Levels on these lines appear as bits 09, 10, and 11 in the Command/Status Register.
ATTN	**Attention.** The signal level on this line becomes bit 13 in the Command/Status Register. ATTN causes an error condition and prevents further bus cycles. If the IE bit is set, ATTN causes an interrupt. If not used, ATTN must be held low.

Table 3. User Device Interface Terms (cont'd.)

Signal	Description
SINGLE CYCLE	When held high, SINGLE CYCLE causes MLSI-DR11B to release bus after each cycle, permitting Unibus to interleave MLSI-DR11B cycles with cycles of other devices. In this case, MLSI-DR11B requests bus master for each cycle. For burst-mode or read-modify-write operations, SINGLE CYCLE is held low, causing MLSI-DR11B to control the bus until SINGLE CYCLE goes high, or until READY is set. Bus cycle does not begin until CYCLE is set.
Outputs from MLSI-DR11B to User Device.	
ODAT00-ODAT15	Data to user device. Data is buffered in Output Data Register, which is loaded under program control, or by an MLSI-DR11 DATI cycle. INIT clears all lines to "0".
INITO	Initialize. Goes high when Q-BUS is initialized.
FNCT1, FNCT2, FNCT3	Function. Bits 01, 02, and 03 in Command/Status Register, output through drivers. Defined by user to control device operation. Cleared by INIT.
READYO	Bit 07 in Command/Status Register. Set high by INIT. Goes low as GO bit is loaded to indicate that a command has been received. Set high again by word count overflow or error.
BUSYO	High level while bus cycle is in progress. Set high as CYCLE is set, and goes low when cycle is complete. When CYCLE is controlled by program, BUSYO follows CYCLE.
END CYCLE O	Positive-going pulse (approx. 100 nsec) output as bus cycle is ended.
GOO	Positive-going pulse (approx. 200 nsec) output as GO is set in Command/Status Register. Indicates start of new operation.

The sequence of operation at the MLSI-DR11B/user device interface is, generally, as follows:

a. The GO bit is set, and READY goes low, indicating that a cycle is to begin. FNCT bits may define the command.

b. The user device then provides the following signals; DATIO0-DATI15, C1 CONTROL, C0 CONTROL, WC INC ENB, and A00IN. These signals must be held on the lines throughout the bus cycle.

c. At least 100 nsec after the data appears on the lines, the trailing edge of CYCLE REQ A or B sets BUSY.

d. At the end of the bus cycle, the MLSI-DR11B sends END CYCLE, and BUSY goes low. A new cycle request will not be serviced while BUSY is set.

The BA INC ENB signal need not be set until BUSY is set. However, BA INC ENB must be held until the end of END CYCLE.

The program may load the CYCLE bit into the Command/Status Register. This raises BUSY, so that a bus cycle is begun when GO is set. Consequently, the MLSI-DR11B is set-up so that the first bus cycle may be begun without a CYCLE REQ (A or B) signal from the user device.

MAINTENANCE

Maintenance Mode Operation

The MAINT bit (bit 12) in the Command/Status Register is for use in diagnostic mode. To configure the MLSI-DR11B as a DRV11B for diagnostic operation (with outputs looped to inputs), a special cable is required between connectors J1 and J2.

The MAINT bit causes the FNCT bits to act as an octal counter which counts bus cycles. Note that with FNCT1 connected to the C1 CONTROL line, the MLSI-DR11B performs alternating DAT1 and DATO cycles. If J1 and J2 are jumpered together but the MAINT bit is not set, either all DAT1 cycles, or all DATO cycles, will be performed.

Because FNCT3 is looped to the SINGLE CYCLE line, the MAINT bit causes a burst mode sequence of four cycles, followed by four single cycles.

Refer to appropriate DEC documentation for details of diagnostics.

SPECIAL LOOPBACK TEST CABLE FOR DRV11B DIAGNOSTIC

J1		J2			J1		J2	
DATI15	1	1	ØDAT15	BA INC ENB	21	21	WC INC ENB	
DATI00	2	2	ØDAT00	GND	22	22	GND	
DATI14	3	3	ØDAT14	INIT V2	23			
DATI01	4	4	ØDAT01	GND	24	24	GND	
DATI13	5	5	ØDAT13	S BUSY	25			
DATI02	6	6	ØDAT02	GND	26	26	GND	
DATI12	7	7	ØDAT12	C1I	27	27	FNCT10	
DATI03	8	8	ØDAT03	GND	28	28	GND	
DATI11	9	9	ØDAT11	STATUS C	29	29	FNCT10	
DATI04	10	10	ØDAT04	GND	30	30	GND	
DATI10	11	11	ØDAT10	STATUS B	31	31	FNCT20	
DATI05	12	12	ØDAT05	GND	32	32	GND	
DATI09	13	13	ØDAT09	SINGLE CYCLE	33	33	FNCT30	
DATI06	14	14	ØDAT06	GND	34	34	GND	
DATI08	15	15	ØDAT08	STATUS A	35	35	FNCT30	
DATI07	16	16	ØDAT07	GND	36	36	GND	
COI	17	19	INITØ	GOØ	37			
AOOI	18	23	READY	GND	38	38	GND	
ATTN	19			CYCLE REQ	39			
GND	20	20	GND	GND	40	40	GND	

Pins not Connected

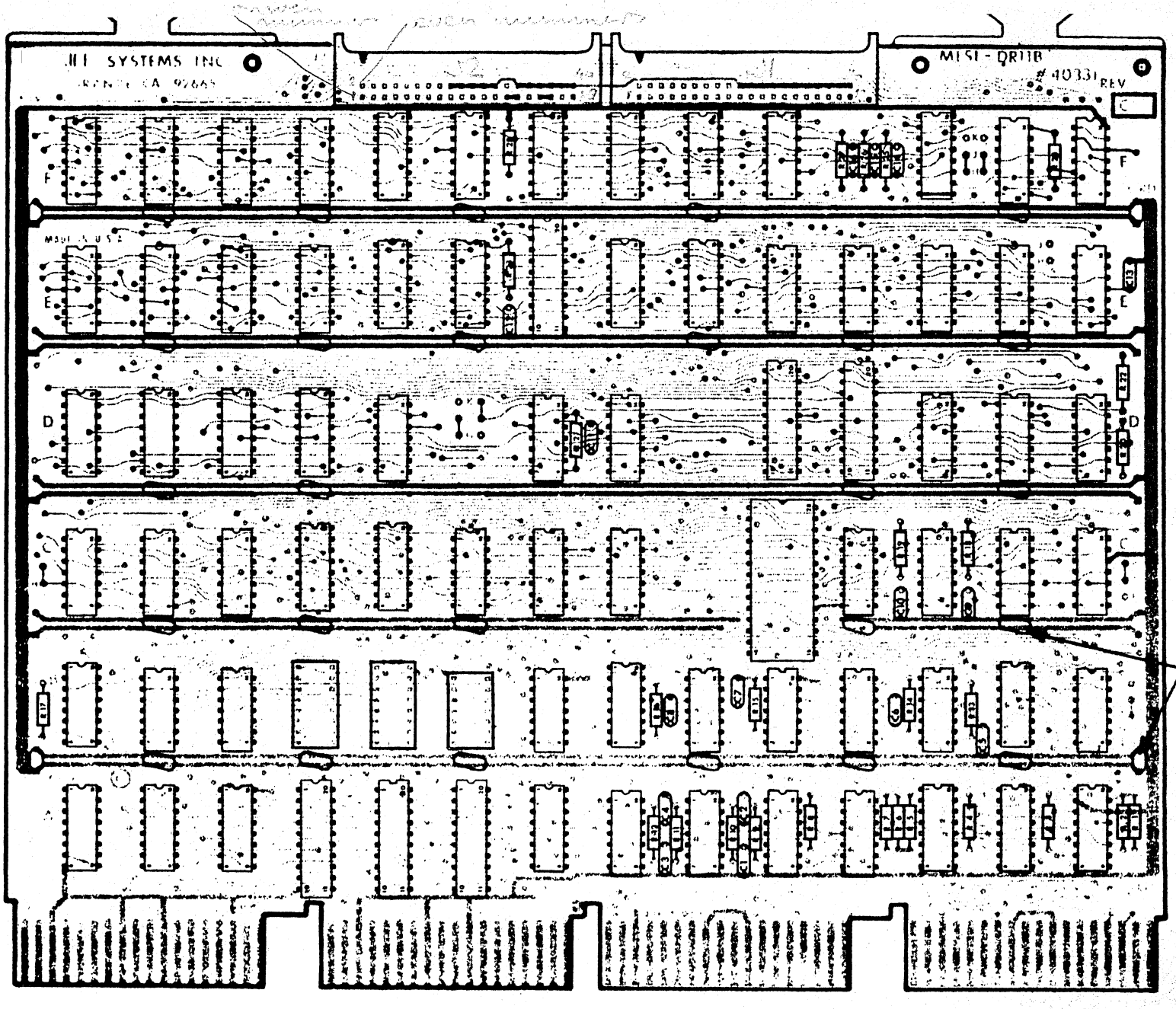
J1 - 37
J2 - 17, -18, -25, -37, -39

Troubleshooting and Repair

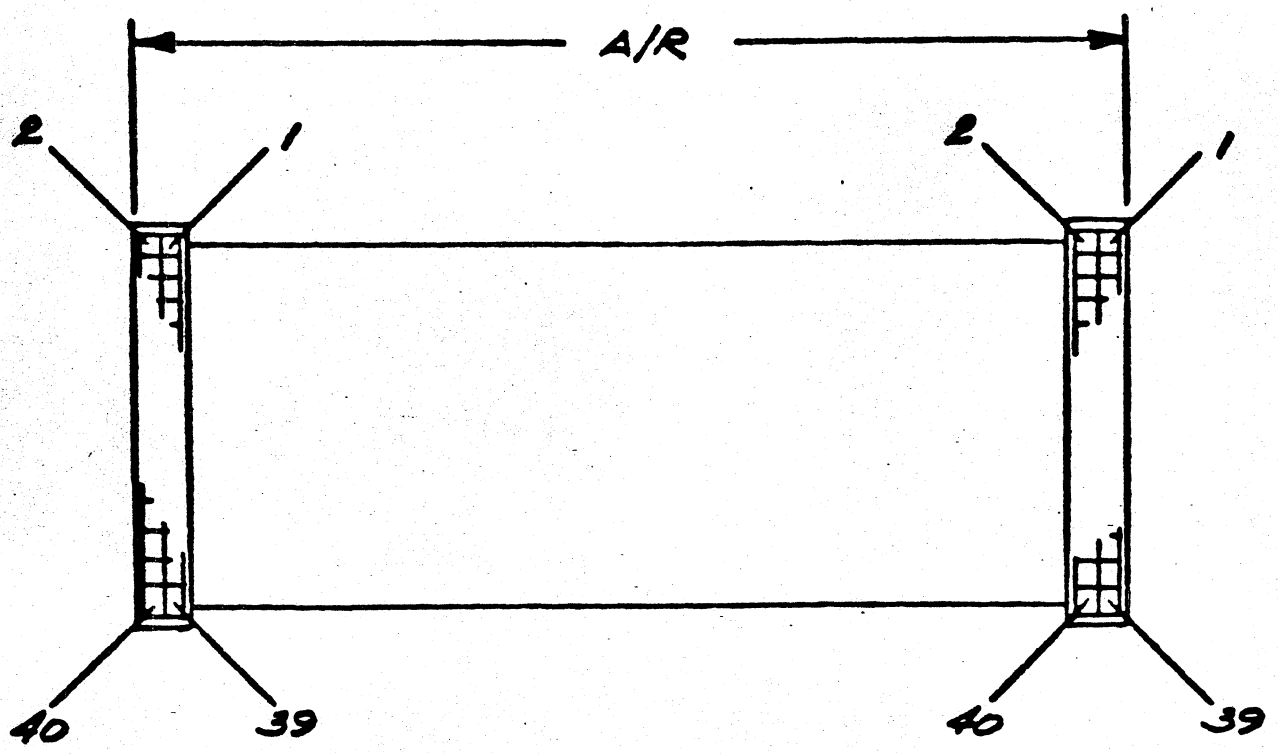
Repair the module using appropriate skills, techniques, and materials. If you wish MDB Systems to repair the module, first notify MDB Systems' Customer Service, then pack the module carefully, along with your best evaluation of trouble symptoms, and ship it, prepaid, to MDB Systems.

Drawings

The following pages contain logic diagrams and assembly drawings useful in maintaining and repairing the module.



COMP. SIDE



CABLE - 40 I/O FLAT RIBBON P/N 171-40
2 40 I/O CONNECTORS, P/N 3M- 3417

CABLE ASSY

MDB SYSTEMS, INC.		
TITLE: GPI/O-40-D		
DATE: JULY 79	SCALE:	
SHEET NO. 1 of 1	DWG. NO. 50046830-XXX	REV.

August 17, 1981

NOTE: This module is not to be used in any DEC model H9273 backplane. The H9273 backplane does not provide any Q-bus signals in Columns C and D.

DRVH1_B

LSI #15